

N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ)
40	0.0038 at V _{GS} = 10 V	33	37.5 nC
	0.0045 at V _{GS} = 4.5 V	31	

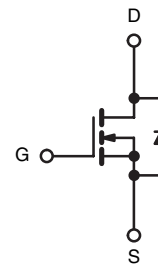
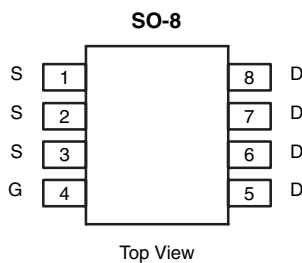
FEATURES

- TrenchFET[®] Gen II Power MOSFET
- 100 % R_g and UIS Tested



APPLICATIONS

- Secondary Rectification
- Point of Load



N-Channel MOSFET

Ordering Information: Si4456DY-T1-E3 (Lead (Pb)-free)

ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V _{DS}	40	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	33
		T _C = 70 °C	27
		T _A = 25 °C	23 ^{b, c}
		T _A = 70 °C	18 ^{b, c}
Pulsed Drain Current	I _{DM}	70	A
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	
		T _A = 25 °C	3.0 ^{b, c}
Avalanche Current	I _{AS}	40	mJ
Single Pulse Avalanche Energy	E _{AS}	80	
Maximum Power Dissipation	P _D	T _C = 25 °C	7.8
		T _C = 70 °C	5.0
		T _A = 25 °C	3.5 ^{b, c}
		T _A = 70 °C	2.2 ^{b, c}
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, d}	t ≤ 5 sec	R _{thJA}	29	35	°C/W
Maximum Junction-to-Foot (Drain)	Steady	R _{thJF}	13	16	

Notes:

- Based on T_C = 25 °C.
- Surface Mounted on 1" x 1" FR4 board.
- t = 5 sec.
- Maximum under steady state conditions is 80 °C/W.

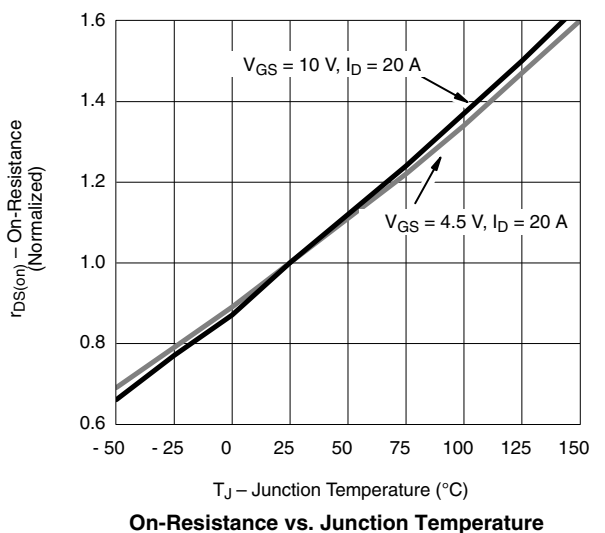
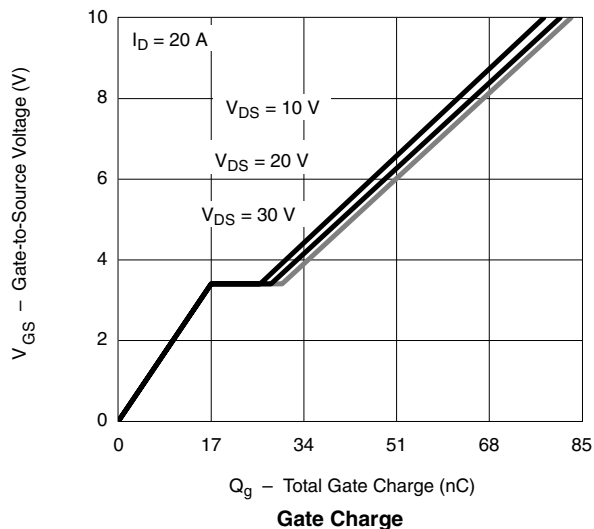
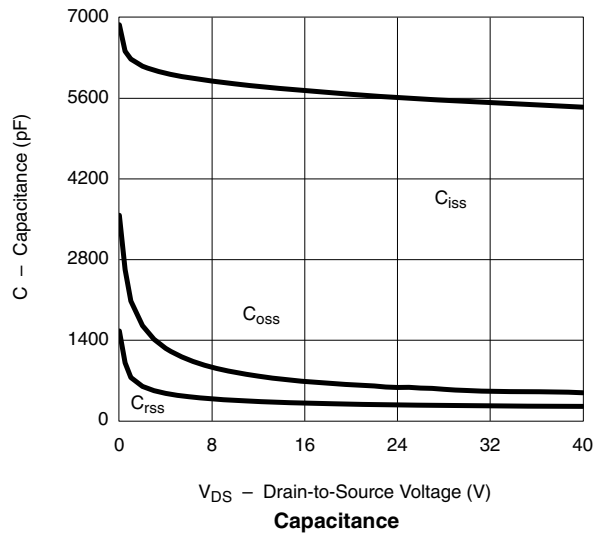
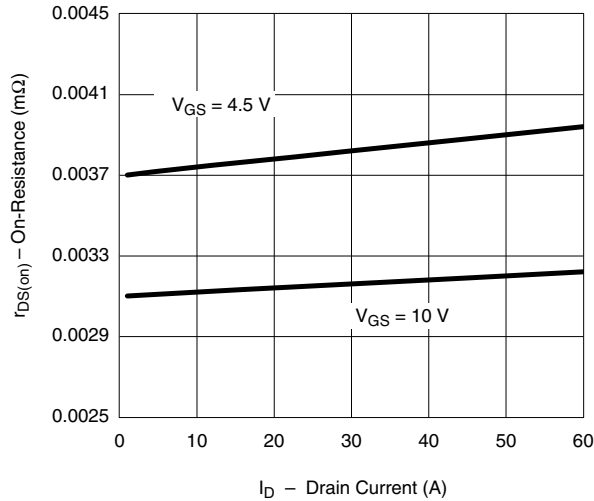
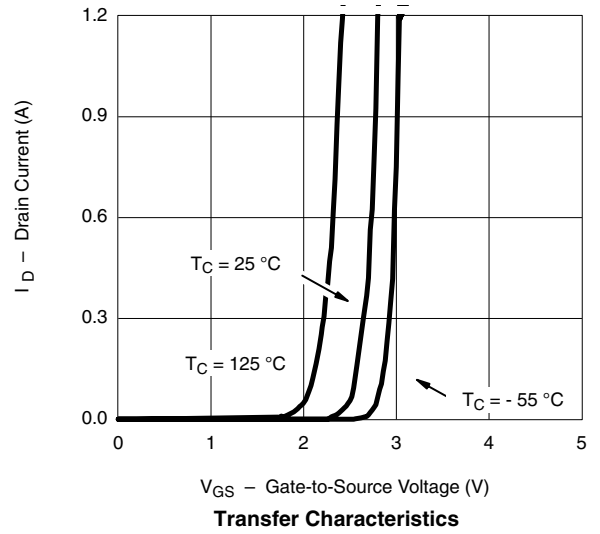
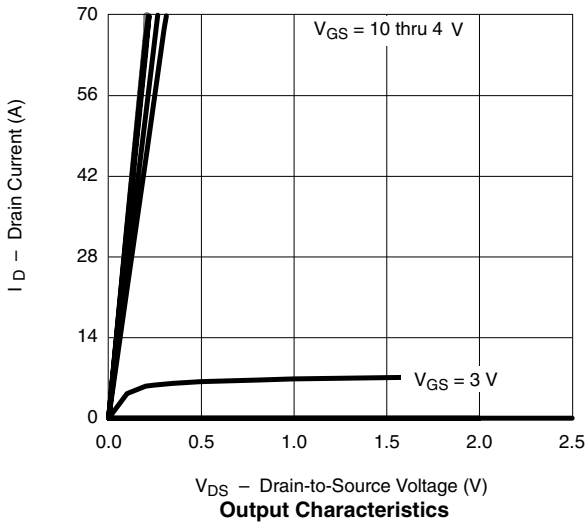
SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	40			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		54		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-7		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.5		2.8	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$			10	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	30			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		0.0031	0.0038	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 15\text{ A}$		0.0037	0.0045	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}$		110		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		5670		pF
Output Capacitance	C_{oss}			621		
Reverse Transfer Capacitance	C_{rss}			287		
Total Gate Charge	Q_g	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 20\text{ A}$		81	122	nC
				37.5	57	
Gate-Source Charge	Q_{gs}	$V_{DS} = 20\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		17		nC
Gate-Drain Charge	Q_{gd}			11		
Gate Resistance	R_g		$f = 1\text{ MHz}$		1.05	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		145	220	ns
Rise Time	t_r			208	320	
Turn-Off Delay Time	$t_{d(off)}$			56	85	
Fall Time	t_f			15	23	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 2\text{ }\Omega$ $I_D \cong 10\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		21	32	ns
Rise Time	t_r			58	90	
Turn-Off Delay Time	$t_{d(off)}$			55	85	
Fall Time	t_f			8	15	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			7	A
Pulse Diode Forward Current ^a	I_{SM}				70	
Body Diode Voltage	V_{SD}	$I_S = 3\text{ A}$		0.71	1.1	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 13\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		38	60	ns
Body Diode Reverse Recovery Charge	Q_{rr}			42	65	nC
Reverse Recovery Fall Time	t_a			21		ns
Reverse Recovery Rise Time	t_b			17		

Notes:

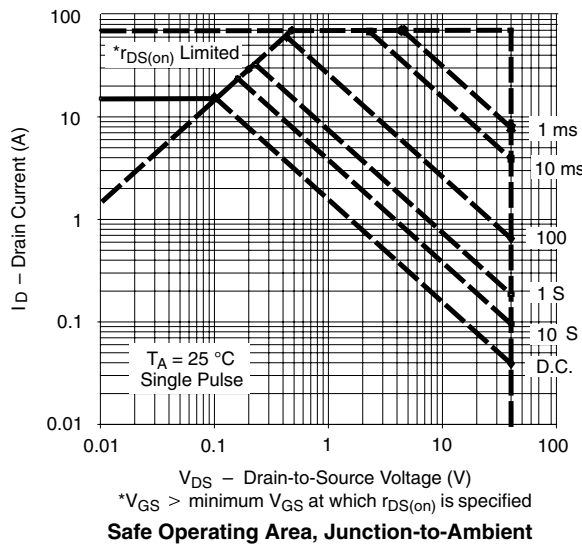
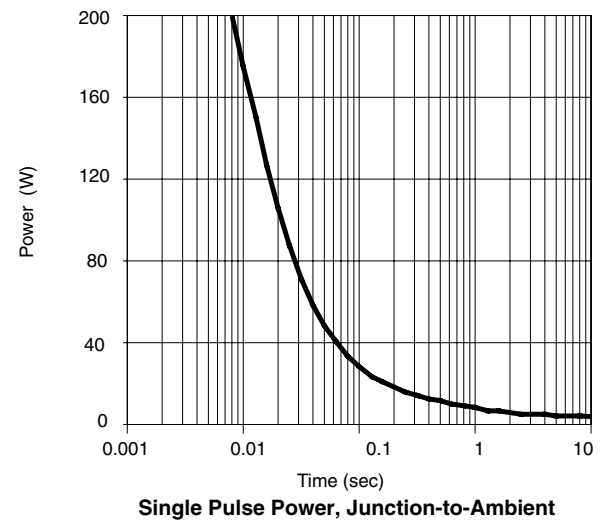
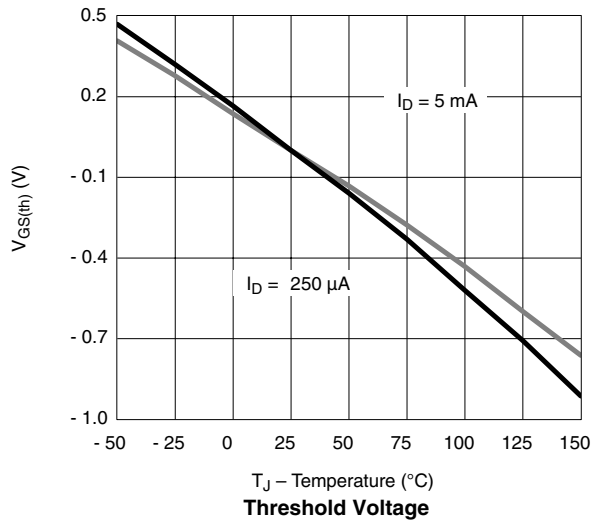
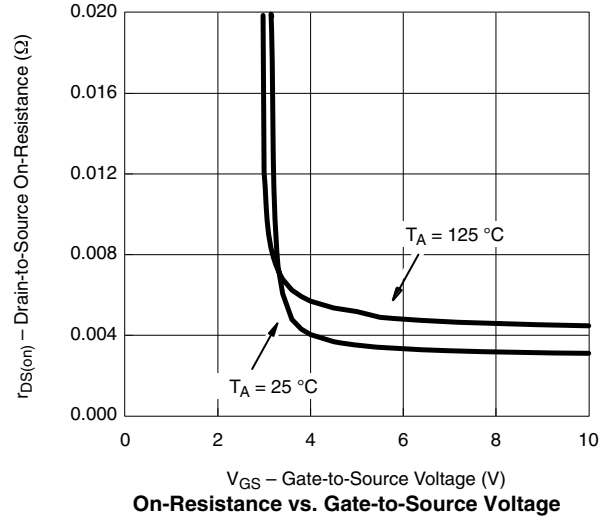
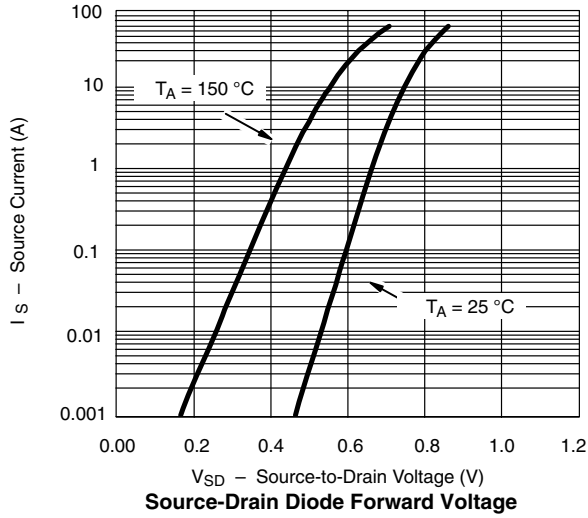
- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

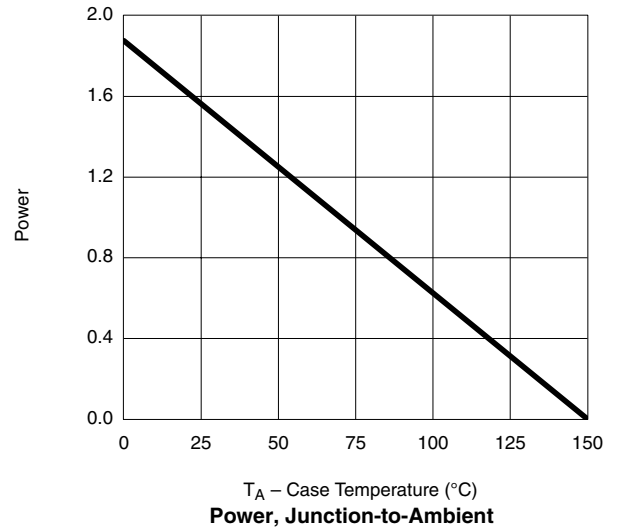
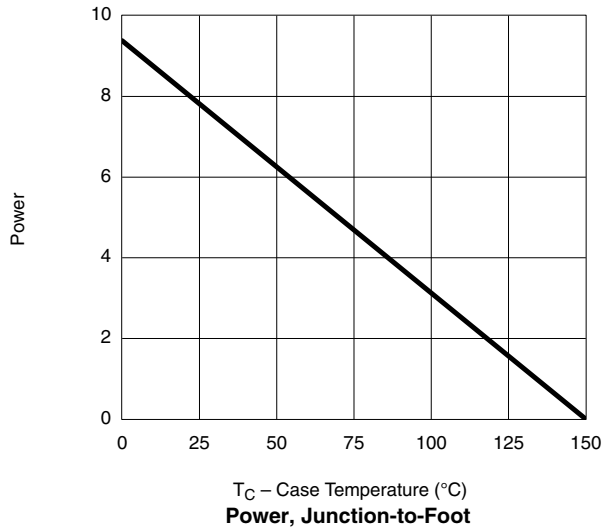
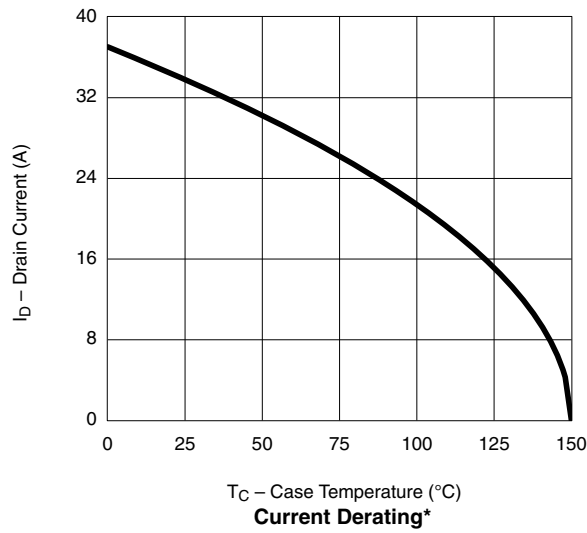
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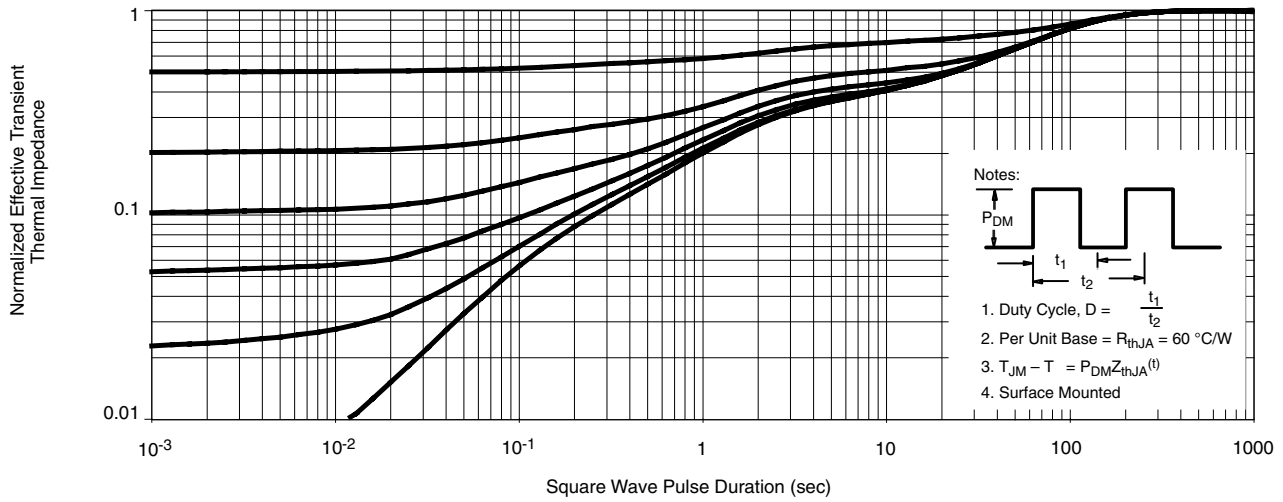


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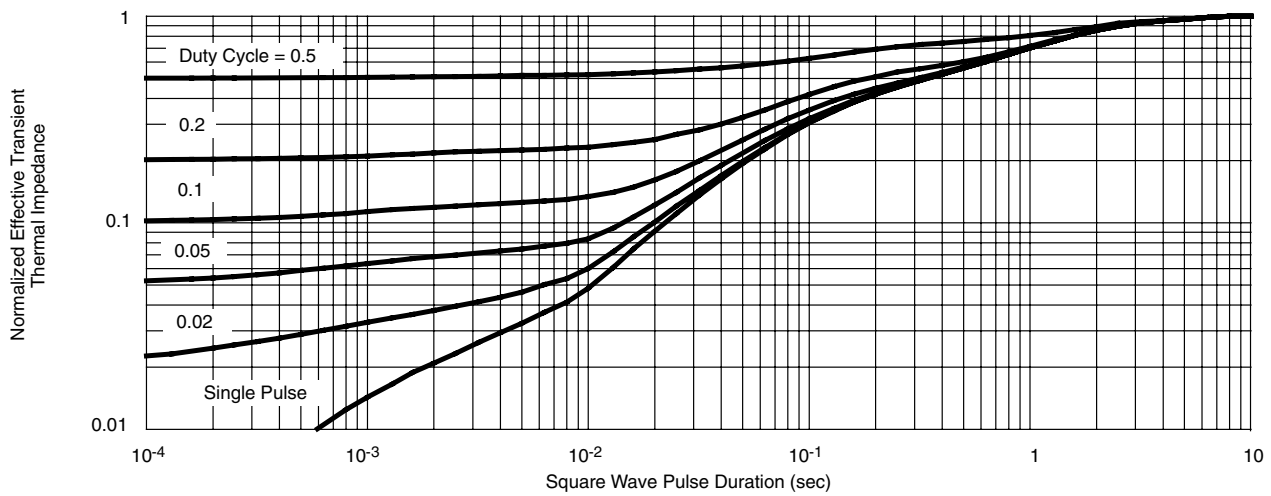


* The power dissipation P_D is based on $T_{J(max)} = 175\text{ }^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS $T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

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